Claims 10-12 remain withdrawn.

With reference to the Office Action, claims 1, 2 and 4-9 stand rejected under 35 U.S.C. 103 as being unpatentable over Eitan (5,768,192) in view of Lee et al. (6,768,165). Claim 3 stands rejected under 35 U.S.C. 103 as being unpatentable over Eitan in view of Lee et al. and further in view of Sadd (6,400,610). Applicants respectfully traverse these rejections in view of the amendments to the claims and the following discussion.

Applicants have discovered that when metal nanocrystals are used as discrete storage elements in memory cells, that both the write/erase speed and the charge retention time can be simultaneously increased by selecting the metal which forms the nanocrystals to have a particular work function value. In doing so, the depth of the potential well at the storage elements is engineered to create an asymmetrical barrier between the substrate and the storage elements, i.e. a small barrier for writing and a large barrier for retention. This is achieved, in the present invention, by using metal nanocrystals as the storage elements with a silicon substrate. Then by carefully selecting the metal work function, the barrier height can be adjusted by about 2 eV, giving a great deal freedom for device optimization.

In contrast to their counterpart semiconductor nanocrystals, metal nanocrystals include higher density of states around the Fermi level, stronger coupling with the conduction channel, a wide range of available work functions, and smaller energy perturbation due to carrier confinement. The higher density of states makes metal nanocrystals more immune to Fermi-level fluctuation caused by contamination, so the metal nanocrystals tend to have more uniform charging characteristics. The wide range of available work functions with metal nanocrystals

provides one more degree of design freedom to select the trade-off between write/erase and charge retention, because the work function of nanocrystals affects both the depth of the potential well at the storage element, or node, and the density of states available for tunneling in the silicon substrate. By aligning the nanocrystal Fermi level to be within the Si bandgap under charge retention conditions and above the conduction band edge under charge erase conditions, fast write/erase and long retention times can be achieved simultaneously in metal nanocrystal memories.

Referencing now new claim 13, this claim combines the elements of canceled claims 1-3 and in addition, specifies that the recited metal nanocrystals are selected to have a work function which facilitates formation of the aforementioned asymmetric potential barriers during writing/erasing and during charge retention. In this manner, the writing/erasing speed and charge retention times are simultaneously increased. Without the use of metal nanocrystals, this functionality could not be achieved because non-metal nanocrystals, such as silicon, for example, cannot allow the necessary "tuning" of the work function

Although Lee et al. suggest the use of metal nanocrystals in storage elements, neither Eitan nor Lee discloses or suggests the foregoing concept of selecting the work function of the metal in the nanocrystals such that the different potential barrier levels for writing/erasing and charge retention are achieved.

In view of the foregoing, Applicants respectfully submit that new claims 13-19 are patentable and allowable over Eitan, Lee et al., Sadd and the remaining references of record. Accordingly, favorable reconsideration of the application is respectfully requested.

Respectfully submitted,

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